IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 7 with the following replacement paragraph:

This application is related to U.S. ~~applications~~ Application No. 10/023,053, "Multi-level Routing Structure for a Programmable Interconnect Circuit," now U.S. Pat No. 6,653,861 ~~Ser. No.~~ [[__]] and U.S Application No. 10/021,844, "I/O Block for a Programmable Interconnect Circuit," now U.S Pat. No. 6,703,860, ~~Ser. No.~~ [[__]] both concurrently filed herewith, the contents of both of which are hereby incorporated by reference in their entirety.

Please replace the paragraph beginning on page 2, line 1 with the following replacement paragraph:

Referring now to FIG. 1, an input/output circuit 10 for an ispGDX.® device couples to a 4:1 multiplexer (Mux) 12 that receives signals A, B, C, and D from four different routing structures, GRP_A, GRP_B, GRP_C, and GRP_D, (not illustrated) respectively. Each routing structure corresponds to a given quadrant (a side of the integrated circuit) for the device. Accordingly, GRP_A receives the input signals from I/O pins 20 in quadrant A, GRP_B receives the input signals from I/O pins 20 in quadrant B, and so on. Input/output (I/O) circuit 10 receives its input signals from its pin 20 and directs them to the appropriate global routing structure on path 19. For example, if I/O circuit 10 is within quadrant A, path 19 would couple to GRP_A.

Please replace the paragraph beginning on page 2, line 10 with the following replacement paragraph:

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Each routing structure is a switch matrix that may receive input signals from selected I/O circuits and programmably route output signals to selected I/O circuits. For clarity, the individual structures are grouped together and jointly designated by a single routing structure 14. A similar device or circuit is disclosed in U.S. Pat. No. 6,034,541, the contents of which are hereby incorporated by reference in their entirety. In addition, each global routing pool has a switch matrix fused by an in-system-programmable non-volatile E^2CMOS® memory bank, configured for one-way routability. A given memory cell in the volatile E^2CMOS® memory bank controls the state of a "fuse point" in the switch matrix. The fuse point may be formed by, e.g., a pass transistor that will programmably connect an input lead of the switch matrix to an output lead of the switch matrix, depending upon the logical state (high or low) of the fuse point's memory cell. I/O pins 20 to the device are arranged in quadrants (the four sides to the chip) such that an individual routing structure receives signals from the I/O circuits 10 in a single quadrant and may distribute these signals to the I/O cells ~~circuits~~ 10 in all four quadrants. Thus, the four input signals A, B, C, and D for each Mux 12 are "quadrant" limited to originate in their respective quadrants. Note that, with respect to routing structure 14, each I/O circuit 10 is independent and separate from the remaining I/O circuits. Because routing structure 14 distributes signals independently to each I/O circuit 10, the resulting arrangement may be denoted as "pin-oriented" or "bit-oriented" in that each I/O circuit 10 associates with a single I/O pin 20.

Please replace the paragraph beginning on page 6, line 17 with the following replacement paragraph:

Each I/O block 32 may ~~receives~~ receive signals from two independent routing structures contained within routing structure 15: a data-path routing structure 34 for programmably routing data signals, and a second control-path routing structure 36 for

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programmably coupling control signals to a control array 56, which in turn provides product-term control signals to block 32. It will be appreciated that although data-path routing structure 34 and the control-path routing structure 36 are independent, such independence may be conceptual only in that the data-path routing structure 34 and control-path routing structure 36 may be combined into a single global routing structure. For example, a single switch matrix may accommodate both data and control signals. However, the fuse patterns within the switch matrix or global routing structure may differ according to whether data signals or control signals are being routed.

Please replace the paragraph beginning on page 13, line 18 with the following replacement paragraph:

Turning now to Figure 8a, the coupling of the product-term control signals from the control array 56 to the I/O cell's registers is illustrated. In addition to the product-term clock and clock enable (CE) signals 70, global clock signals 105 are also distributed to the registers. To control clock skew and permit clock synthesis, each global clock signal 105 is associated with a phase-locked loop (PLL) 100 (Figure 2). Thus, should there be four global clock signals 105, there will be four PLLs 100. Further details regarding PLLs 100 are described in co-pending U.S. Application No. 10/021,873, now U.S Patent No. 6,661,254, "Programmable Interconnect Circuit with a Phase-Locked Loop," ~~U.S. Ser. No.~~ [[__]], concurrent filed herewith, the contents of which are hereby incorporated by reference. Global clock signals 106 couple to programmable interconnect device 25 through dedicated pins (not illustrated). From these dedicated pins, global clock signals 105 are distributed to the I/O circuits 16 through a clock tree (not illustrated) independently of the routing structure 14. The clock and CE input to each register 90, 92, and 94 in I/O circuit 16 couples through a clock MUX 120 that selects between the global clock signals 105 and the product-term clock and clock enable

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(CE) signals 70. MUXes 110 provide ~~provides~~ polarity control for the output signal of clock MUXes 120. A clock MUX 120 may be common to both clock inputs of the OE register 94 and output register 92. Similarly, a clock MUX 120 may be common to both CE inputs of the OE register 94 and output register 92. However, as the dashed line 130 indicates, the polarity MUXes 110 provide individual control for these inputs despite their common origin at the clock MUXes 120.

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